PCT

(51) International Patent Classification 5 : G06F 15/46	**A1**	(11) International Publication Number: **WO 94/00824**
		(43) International Publication Date: 6 January 1994 (06.01.94)

(71) Applicant: SQUARE D COMPANY [US/US]; 1415 South Roselle Road, Palatine, IL 60067 (US).

(72) Inventors: REID, Drew, A. ; 9101 Demery Court, Brentwood, TN 37027 (US). BILAS, Ronald, J. ; 4405 Orchard Avenue, Cedar Rapids, IA 52405 (US).

(74) Agent: GOLDEN, Larry, I.; Square D Company, 1415 South Roselle Road, Palatine, IL 60067 (US).

(54) Title: COMPUTER-CONTROLLED CIRCUIT BREAKER ARRANGEMENT WITH CIRCUIT BREAKER HAVING IDENTIFICATION CIRCUIT
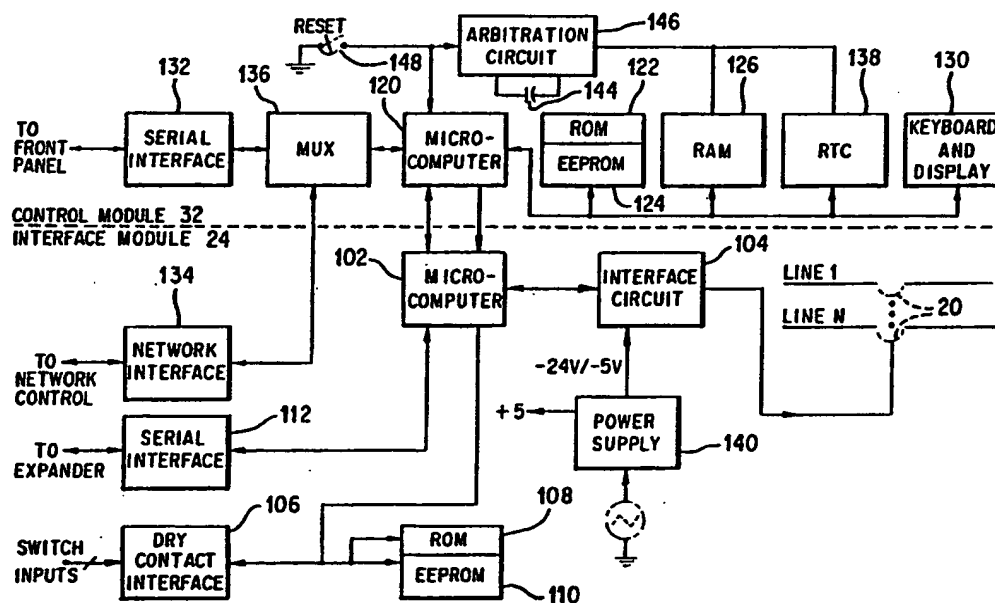
(57) Abstract

An energy management load panel arrangement includes a load panel enclosure (10) having a plurality of circuit breakers (20), each of which opens and closes in response to a control signal so as to interrupt an associated current path. A microcomputer (120) generates the control signals to control the position of the circuit breakers (20) and their associated current paths. The circuit breakers (20) include a digital code circuit which is manually set to indicate the type of circuit breaker, for example, a one, two or three pole circuit breaker.

1

COMPUTER-CONTROLLED CIRCUIT BREAKER ARRANGEMENT
WITH CIRCUIT BREAKER HAVING IDENTIFICATION CIRCUIT

Related Application

This is a continuation-in-part of U.S. Patent Application Serial No. 07/723,370, filed on June 28, 1991 and entitled ELECTRICAL DISTRIBUTION SYSTEM HAVING MAPPABLE CONTROL INPUTS,

5   incorporated herein by reference.

Field Of The Invention

The present invention relates generally to circuit breaker tripping systems, and, more particularly, to microcomputer-based

10   circuit breaker energy management systems in which the circuit breakers open and close in response to a control signal from a computer.

Background Of The Invention

15   Circuit breaker energy management systems are designed to control circuit breakers in a circuit breaker panelboard by commanding the circuit breakers to turn "on" and "off," so as to "close" and "open" the current path for efficient energy use. Typically, a microcomputer is programmed to generate such commands.

20   It is advantageous for such systems to be user-programmable and user-maintainable so that circuit breakers in the panelboard can be replaced and additional circuit breakers can be added to the system. In a newly installed system having all two-pole breakers, for example, the microcomputer would be programmed to control only

2

two-pole circuit breakers at designated circuit breaker positions,
or slots, in the panelboard. If the panelboard subsequently
required, after initial installation, a three-pole circuit breaker,
the program for the microcomputer would have to be replaced so that
5   the microcomputer can communicate with, and properly control the
newly added circuit breaker.

        This type of adaptability is not only burdensome and expensive
for the user, it is unacceptable in many applications in which
accessibility is difficult or prohibited.   Accordingly, a
10   microcomputer-based circuit breaker energy management system is
needed which overcomes these deficiencies of the prior art.

Summary of Invention

        The present invention provides an energy management loadpanel
15   arrangement including a loadpanel enclosure having a plurality of
circuit breakers, at least one of which includes a digital circuit
indicating the type of circuit breaker (for example, one, two or
three pole) and which opens and closes in response to a control
signal generated by a microcomputer.

20   In a particular embodiment, an energy management loadpanel
arrangement includes a loadpanel enclosure and a plurality of
circuit breakers secured in the enclosure. At least one of the
circuit breakers is digitally-coded and capable of opening and
closing in response to a control signal so as to interrupt an
25   associated current path. A microcomputer responds to the digital
signal by determining the type of circuit breaker represented by

3

said digital signal and then generates the control signal to control the circuit breaker and its associated current path. Thus, the digital signal is used by the microcomputer to determine the identity, or type, of circuit breaker disposed at one or more of

5   the circuit breaker positions in the loadpanel.

The circuit breaker that is digitally-coded includes an interface circuit that provides the data to the microcomputer serially, using only two lines. One of the lines is used to select (or activate) the interface circuit, and the other line is used to

10   generate a clock pulse in one direction and to read the digital signal in the other direction. In an application requiring a multitude of circuit breakers each having a respective identification circuit, this two-line communication scheme is used in an array to provide access to the respective interface circuits

15   of all the circuit breakers.

Brief Description Of The Drawings

Other advantages of the invention will become apparent upon reading the following detailed description and upon reference to

20   the accompanying drawings, in which:

FIG. 1a is a perspective view of a load center arrangement, according to the present invention;

FIG. 1b is another perspective view of the load center arrangement of FIG. 1a;

25   FIG. 2 is a block diagram of the control module and interface module shown in FIGS. 1a and 1b;

4

FIG. 3 is an expanded block diagram of a portion of the interface module of FIG. 2, illustrating a manner in which a microcomputer of the interface module can efficiently communicate with the circuit breakers through an interface circuit;

5   FIG. 4 is a schematic diagram of one of several motor driver circuits illustrated in FIG. 3;

FIG. 5 is a schematic diagram of one of several circuit breaker select driver circuits illustrated in FIG. 3;

FIG. 6 is a schematic diagram of the electrical portion of a

10   circuit breaker illustrated in FIG. 1a;

FIG. 7 illustrates a circuit breaker, according to the present invention, which may be used as part of the arrangement shown in FIGS. 1a and 1b; and

FIG. 8 is a state diagram depicting the power driver, data

15   transmit and data receive operations of the gate array illustrated in FIG. 3.

While the invention is susceptible to various modifications and alternative forms, a specific embodiment thereof has been shown by way of example in the drawings and will herein be described in

20   detail. It should be understood, however, that it is not intended to limit the invention to the particular form disclosed, but on the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

25

The Best Mode For Carrying Out The Invention

The present invention has direct application for managing
energy by monitoring and interrupting current paths passing through
a panelboard (or circuit breaker box), according to specifications

5   that may be programmed by the user. For example, it may be
desirous to program the panelboard so that certain types of circuit
breakers open and close at specified times of the day. In this
way, the energy provided through the panelboard can be efficiently
used.

10   The panelboard arrangement of FIGS. 1a and 1b provides an
extremely adaptable and user-friendly panelboard, in which a
panelboard or load-center enclosure 10 distributes, from a
plurality of input power lines 12, power to various loads (not
shown) via lines 14 which exit the enclosure 10. Bus boards 16 and

15   18, which may be implemented on the same board, are disposed in
parallel on each side of the load-center for mounting remotely
controlled circuit breakers 20, each having a plug-in socket which
is coupled to one of a plurality of connectors 22 on the bus boards
16 and 18. The connectors 22 are used with the bus boards 16 and

20   18 to carry motor control and contact-status signals, via an
interface module 24, to and from the circuit breakers 20. The
interface module 24 interprets messages from a controller (or
control module) 32 so as to facilitate electrical control and
monitoring functions from both local and remote locations.

25   As illustrated in the block diagram of FIG. 2, the circuit
breakers 20 are controlled by a microcomputer 102, which is part of

the interface module (24 of FIG. 1) depicted below the dashed
lines. Between the circuit breakers 20 and the microcomputer 102
there resides an interface circuit 104 which preferably includes an
optical isolation circuit (not shown) to isolate the circuit
breakers 20 from the remainder of the interface module.

Various types of circuits can be used to implement the
interface circuit 104. For example, the I/O bits from the
microcomputer 102 can be used so as to directly drive the inputs of
the optical isolators. Alternatively, a modified version of the
gate array circuit disclosed in "ELECTRICAL DISTRIBUTION SYSTEM
WITH IMPROVED CIRCUIT FOR MULTIPLE CIRCUIT BREAKER CONTROL", supra,
can be used to implement the interface circuit 104. Such a gate
array is described in connection with FIGS. 3 et seq.

The microcomputer 102 commands the circuit breakers to their
respective "open" and "closed" positions according to respective 2-
wire or 3-wire switch inputs provided at a dry contact interface
106. The connections for, and control over, the signals at the
switch inputs can be implemented as set forth in the last-
referenced application, or using conventional methods, such as the
implementation in Square D Company's "PowerLink" product, or as
described in U.S. Patent Application No. 07/620,237, filed on
November 29, 1990 and entitled "Power Management and Automation
System." Alternatively, the circuit breakers 20 are controlled via
a program stored by the microcomputer 120.

The microcomputer 102 uses conventional memory circuits, for example ROM 108 and EEPROM 110, for storage of its object code and other data requiring permanent or semi-permanent preservation.

As an option, the interface module can also include a serial interface circuit 112 to permit the microcomputer 102 to communicate with similarly situated panelboard arrangements, such as the one shown in FIGS. 1a and 1b.

The control module (32 of FIG. 1b and shown above dashed lines in FIG. 2) incorporates a microcomputer 120, and conventional memory circuits including ROM 122, EEPROM 124 and RAM 126, to provide the overall control for the panelboard arrangement. This control includes overall initialization, communication between the microcomputers 120 and 102, monitoring and control of the keyboard and display 130, and I/O communication via a serial interface 132 or a network interface 134. A multiplexer 136 is used to establish which interface 132 or 134 communicates with the microcomputer 120.

The keyboard and display 130 can be implemented using conventional LCD type driver and key read circuitry. For example, a 44 character by 8 line display and a 24 button push key circuit can be used to provide status-reading and function-programming capabilities to a user.

The ability to control the circuit breakers 20 according to the time of the day is established by a program entered via the keyboard and display 130. The microcomputer 120 employs a conventional real time clock (RTC) 138, such as the DS1283S available from Dallas Semiconductor, to maintain the time.

8

The entire panelboard arrangement of FIG. 2 is provided power via a conventional power supply 140, including a regulated Vcc (+5 Volts and associated common), a separately regulated +5 Volt Isolated ("VISO" and associated VISO common), and separately

5   regulated -24 Volt and -5 Volt outputs sharing a common ground.

The power supply 140 is preferably sourced by a 240 volt AC or 480 volt AC line and, therefore, is susceptible to long-term interruptions. These long-term power interruptions, for example, are frequently encountered with electric company overloads,

10   blackouts and other events requiring manual service or repair by the electric company. Thus, during these interruptions a secondary power supply is needed to maintain the integrity of important data which is used frequently and is not stored in the non-volatile EEPROM.

15   The secondary power supply is provided using an electrical double-layer capacitor (EDLC or SUPERCAP) 144, which supplies secondary power to the RTC 138 and RAM 126 via a power arbitration circuit 146. The arbitration circuit 146 ensures that a +5 Volt source supplies power to the RTC 138 and RAM 126 either from the

20   power supply 140 or from a stored capacitive charge on the EDLC 144. Thus, in the event that the power supply 140 shuts down, each of the circuits shown in FIG. 2 powers down except for the RTC 138 and RAM 126 (and unshown logic support circuits), which stay powered up as long as there is sufficient charge on the EDLC 144.

25   An FS or FE type SUPERCAP available from NEC Corporation, which may

be used for this application, provides several weeks of standby power for the implementation shown in the figures.

A reset switch 148 is used to reset the entire circuit of FIG. 2 via its connection to both the microcomputer 120 and the arbitration circuit 146.

Other aspects of the EDLC 144 and the RTC 138 are discussed in copending U.S Patent Application No. _____, entitled "COMPUTER CONTROLLED ENERGY MANAGEMENT ARRANGEMENT HAVING RELIABLE MEMORY AND CLOCK," filed concurrently herewith and assigned to the instant assignee. This application is also incorporated herein by reference.

Communication between the microcomputers 102 and 120 can be provided using any of a number of asynchronous or synchronous serial communication schemes. For example, synchronous communication can be provided using three lines which directly interconnect the microcomputers and establish the control microcomputer 120 as the master and the interface microcomputer 102 as the slave. Using Intel's 80C31B type microcomputers, for example, the P1.0 port for the master 120 and P1.4 port for the slave can be used as the data in/out line ("DATA"), the P1.1 port as an input for the master 120 and P1.5 port as an output for the slave can be used as the handshake line for the interface microcomputer 102 ("I.HS"), and the P1.2 port as an output for the master 120 and the INT1 port as an input for the slave can be used as the handshake line for the interface microcomputer 102 ("C.HS"). In such an implementation, the command/response format would be

10

initiated by the master, by sending an OP-CODE type command
followed by the number of data bytes to be sent, and followed by
the data bytes and a checksum word. The response would be a
response number, followed by the number of data bytes to be
5   returned, and followed by the data bytes and a checksum word.

Error checking between the master and slave is also provided
using a software watchdog timer in each microcomputer.

Appendix A, attached hereto, illustrates the timing of the
communications between the microcomputers 102 and 120.

10   Fig. 3 illustrates the interface circuit 104 providing the
control, and reading, of the circuit breakers 20 under control of
the microcomputer 102 of FIG. 2. From the microcomputer, data is
transmitted to and received from a gate array 206 serially, via an
optical isolator 210. The gate array 210, which can be implemented
15   using a semi-custom part available from ACTEL, Inc. of Sunnyvale,
California, is provided a clock signal by a conventional
oscillation circuit 216 operating, for example, at 455 kHz. The
optical isolator 210 can be implemented using two NEC2501-1 type
parts with respective resistors (R = 1k Ohm) providing the
20   appropriate bias at the inputs and outputs of the optical isolator
210.

The serial communication between the microcomputer and the
gate array 206 is performed using a sixteen bit word, the bits of
which are as follows (beginning with least significant bit):

25   first nine bits: six address bits followed by three
command bits;

11

tenth and eleventh bits: fixed bits at 0 and 1, respectively, for error detection;

next four bits: check bits using a hamming code;

last bit: fixed stop bit at 1.

5   There are five commands implemented in the three command bits. They are: 001 - open, 101 - close, 010 - read motor status, 110 - read contact status, 100 - read ID circuit, and 000 - NO OP. The NO OP command is used to read the transmit buffer in the gate array without communicating with the circuit breakers. The transmit

10   buffer in the gate array is automatically read whenever one of the other commands is sent to the gate array.

The gate array 206 feeds six circuit breaker row drivers 212 and seven circuit breaker column drivers 214, which are configured seven down and six across, respectively, for controlling the motors

15   "M" and identification circuits "ID" of up to forty-two circuit breakers. Each of the circuit breaker row drivers 212 and circuit breaker column drivers 214 acts as an amplifier to the corresponding signal from the gate array 206.

Each row driver 212 is used to select (or enable) the circuits

20   of six circuit breakers, while each column driver 214 is used to actuate the circuit breaker motor and identification circuit pair which is selected by the intersecting row driver 212.

A status filter 220 is connected to the circuit breakers in each row in order to receive a status signal from a particular

25   circuit breaker. The status signal is used to report whether the contacts of the circuit breaker are open or closed. The status

12

signal from a circuit breaker is operative, and readable via the
gate array 206, when two conditions are present: the corresponding
column driver 214 is selecting the column of circuit breakers in
which the status filter 220 is associated; and the gate array 206
5   is actuating a triac circuit (e.g., a Siemens IL420) 218 to
provide, simultaneously, a momentary common path (LED COMM on the
bus boards 16 and 18 of FIG. 1a) for the input ports of the optical
isolators 230 (FIG. 6) of all forty-two of the circuit breakers.
The gate array 206 then reads all six statuses and determines which
10   of these statuses are to be sent to the controller 32. The circuit
breaker contacts are preferably monitored using a lead 231 (FIG. 6)
connected to the load terminal of the circuit breaker 20.

A varistor 222, such as a GE-V30DLA2, is coupled across the
output ports of the triac circuit 218 to provide circuit protection
15   against voltage and current transients.

In FIG. 4, the column (or motor) driver 214 is shown as being
controlled by the gate array 206 using CDa, CDb and MSTAT leads so
as to drive the motor on the selected circuit breaker 20. The
diodes 232 through which the motor drive signal passes are located
20   on the bus board 16 or 18 to allow a current path through only one
circuit breaker 20. The CDa and CDb signals from the gate array
206 are controlled in a polarized manner between -5 Volts and
common so that if either signal is absent, the designated circuit
breaker 20 cannot be commanded to open or close its contacts.

25   The MSTAT signal is used to indicate whether or not a motor is
present. This type of status check operates in substantially the

same manner as the statuses from the associated circuit breaker
load, as described above. The MSTAT signal is operative when the
corresponding column driver 214 selects the column of circuit
breakers associated with the circuit breaker under test. The gate
5   array 206 then reads all six MSTAT signals and determines which of
these signals are to be sent to the controller 32. A diode 235 is
connected between -24 Volts and "OPEN" to prevent the signal level
on "OPEN" from falling below this point, a pull-down resistor 236
is connected between -5 Volts and "CLOSE" to maintain the signal at
10   -5 Volts when it is not being driven by the designated circuit
breaker.

In FIG. 5, the row (or select) driver 212 is shown as being
controlled by the gate array 206 using RDa and RDb leads so as to
select the appropriate row of circuit breakers 20. The diodes 238
15   and 239 are used to mitigate the effect of transient signals
received from the bus boards 16 and 18.

FIG. 6, which illustrates the electrical control portion of
the preferred remote control circuit breaker 20, depicts six leads
carried by each plug-in connector (22 of FIG. 1a) of the bus boards
20   16 and 18. The first four of these include: the select lead 246,
status lead 248, motor drive lead 250 and an isolator enable lead
252. The signals of each of these leads are carried on the bus
boards 16 and 18 (FIG. 1a) using the six-by-seven array
configuration of FIG. 3 to limit the number of conductors required
25   to communicate with the circuit breakers.

14

A parallel resistor/diode arrangement 254/256 serves two functions. The diode 254 may be used to provide current flow in a unilateral direction, while the resistor 256 is used to control the power provided from lead 258 to the motor of the circuit breaker

5   20. The value of the resistor 256 is selected according to the necessary current specified to operate the motor. In the event that the lead 258 is used to control a plurality of poles, e.g., for controlling two or three circuit breaker poles, the resistance required will vary. For single pole operation by a FK130S-10300

10   Mabuchi motor, the value of the resistor 256 is preferably 12 Ohms.

The remaining two leads carried by each plug-in connector, data/clock 262 and -5 Volts 264, are used in combination with select 246 to control and access the identification portion of the circuit in the circuit breaker. This configuration allows the

15   transmission of encoded digital information from the gate array to as many as forty-two conductors using a limited number of conductors, using conventional parts and using no internal clock.

Each of nine status bits, which are manually settable at JMP1- JMP9 positions, are converted to serial data at lead 272 using a

20   74HC165 shift register 273 so as to permit up to 256 digital signals to be read by the gate array. These signals can be used to indicate how many poles the circuit breaker includes, the current rating of the circuit breaker, and other information that is associated with the circuit breaker or with the circuit breaker

25   position. For example, the controller can determine if there exists a circuit breaker in a particular circuit breaker position

15

by using all "0"s to indicate that no circuit breaker is present, and another code to identify the type and/or status of a device in that position that is not a circuit breaker, for example, a plug-in surge protector. Other possibilities exist as well.

5   The identification circuit remains inactive while power is off and presents a high impedance to any circuitry connected to the clock/data lead under these conditions. When select 246 is either open circuited or taken to the same voltage potential as -5 Volts 264, transistors 266-268 are inactive and data/clock 262 appears as 10   a high impedance input to external circuitry. A 1000 Ohm resistor 269 bleeds off any charge from between Vcc and -5 Volts, and a diode 270 discharges capacitor 271 in preparation for when power is next applied to select 246.

Power is applied between select 246 and -5 Volts 264 by 15   setting select 246 to 0 Volts. When this occurs, capacitor 271 will be discharged and will hold SH_LD input of the shift register 273 low for a short time causing the data present at SER and A-H inputs to be parallel loaded into the shift register 273. Also during this initialization phase, transistors 266-268 will be 20   enabled and the voltage at data/clock 262 (set to "high" at initialization) will appear at the collectors of transistors 266 and 267. After stabilization of the initialization phase, the CLK input of the shift register 273 will be high and its SH_LD input will also be high allowing the shift register 273 to enter its 25   shift mode of operation. At this point, the data present at the H input will be present at QH output of the shift register 273. A

16

100 kOhm resistor 280 acts to hold the power on the shift register
down until select 246 reaches 0 Volts.

        To transmit data from the shift register 273, a specific
sequence of events is used. To read the first bit present at QH,

5   all that is required is to tri-state data/clock 262. If the data
present at QH is a "1", QH will hold the line high through a 1000
Ohm resistor 274. If the data present at QH is a "0", data/clock
262 will be pulled low through the resistor 274. In either case,
the data present in the shift register 273 will not be shifted

10   because its clock requires a low-to-high transition to shift the
data.

        To shift the next data bit to the QH output, the first step
is to take data/clock 262 from tri-state to low. This action has
no effect on the clock input of the shift register 273. If QH is

15   low, it will remain low; if it is high, it will be pulled low
because data/clock 262 will over-drive the QH output through the
resistor 274. In either case, the shift register will not have
been clocked yet.

        The next step is to drive data/clock high. This will drive

20   the clock input high and cause a data shift regardless of the state
of QH. The data is then read by tri-stating the data/clock and
reading the data present at QH via the resistor 274 and the
transistors 266-267. If QH is high, data/clock 262 will simply
remain high; if it is low, data/clock 262 will go low. In either

25   case the data in the shift register will not be inadvertently
shifted.

The SER input to the shift register 273 is set for odd or even parity to provide error detection.

Accordingly, each of the data bits at JMP1-JMP9 is shifted and read by tri-stating the data/clock, reading the data present at QH and then taking data/clock 262 from tri-state to low for the next data bit.

For further details concerning the configuration of the gate array of FIG. 3, a two-sheet schematic, representing the detailed electrical configuration of the gate array of FIG. 3, is attached hereto as appendix B. Also, a one-sheet schematic identifying the pinout/interface configuration for the gate array of FIG. 3 is attached hereto as appendix C. The pinout list for the gate array is listed in appendix D.

An implementation for the circuit breaker 20 is shown in expanded form in FIG. 7. The arrangement includes an insulative body or housing 310, a line terminal 314 and a load terminal 316 for completing the circuit between the source and load (not shown). More specifically, the circuit path beginning at line terminal 314 carries current through stationary and movable contacts 318 and 320 and through a flexible copper conductor 322, which is soldered between a carrier 324 and a bimetal 328. A rigid conductive plate 329 carries current from the bimetal 328 to the load terminal 316.

Remote control is provided using a motor 350 having a shaft 352 which rotates in one direction to pull the carrier 324 and break the current path and which rotates in the opposite direction to allow the carrier 324 to be pulled by spring 334 to re-establish

the current path. This is accomplished with a shaft spring 354
which is mounted around the shaft 352, and a gear 356 which rotates
about a pin 357 to control a hook-shaped drive rod assembly 358
which includes an end which bends into a hole 325 in the contact

5   carrier 324 for pulling the carrier 324. The shaft spring 354 is
secured at one end 360 to the shaft 352, using a torsional-type
pressure fitting, so that the shaft spring 354 rotates with the
motor shaft 352. The gear 356 includes teeth 362 which interlock
with the windings of the spring 354 to establish a linear

10   relationship between the rotation of the shaft 352 and the rotation
of the gear 356 about pin 357. For example, clockwise rotation of
the shaft 352 may correspond to a counterclockwise rotation of the
gear 356 about pin 357.

A coupling pin 364, which is secured to and protrudes out of

15   the gear 356, responds to the rotation of the gear 356 to control
the position of the contact carrier 324. As the gear teeth 362
move with the shaft spring 354, the side of the gear 356 opposite
the teeth 362 rotates to the same degree, thereby forcing the
coupling pin 364 to rotate about pin 357. The movement of the

20   coupling pin 364 in the counterclockwise direction pulls the drive
rod assembly 358 a, b to the right in order to pull the contact
carrier 324 away from the stationary contact 318. The drive rod
assembly 358 a, b is sufficiently long to provide a gap on the
right side of the coupling pin 364 when the gear 356 is fully

25   rotated clockwise so that the contact carrier 324 does not prevent
the contacts 318 and 320 from closing.

In response to the motor operating in the opposite direction, the coupling pin 364 rotates in the clockwise direction and allows the biasing spring 334 to return the contact carrier 324 to the contacts-closed position.

5   The circuit of FIG. 6 can be implemented on the printed circuit board 412, or the upper and lower halves of the circuit of FIG. 6 can be mounted on separate printed circuit boards and "piggy-backed" together. A conventional six-pin connector 410 is used to mate the circuit breaker with the bus board 16 or 18 of

10   FIG. 1a.

For additional information concerning the operation and structure of this circuit breaker, reference may be made to copending U.S. Patent Application Serial No. 07/722,050, filed June 28, 1991, entitled "REMOTE CONTROL CIRCUIT BREAKER, and assigned to

15   the instant assignee.

FIG. 8 illustrates, in state diagram form, the power driver, data transmit and data receive operations of the gate array of FIG. 3. The diagram includes eight states, depicted A-H. Beginning at state A, the gate array waits for a command from the controller.

20   The command may be any one of the commands previously discussed: a close contacts command which instructs a particular circuit breaker to close its contacts, depicted by the sequence of states A-B-D-E-A; an open contacts command which instructs a particular circuit breaker to open its contacts, depicted by the sequence of

25   states A-C-D-E-A; a read contacts command to determine if a particular circuit breaker's contacts are closed or open, depicted

by the sequence of states A-E-A; a read motor command to determine
if the motor is present, depicted by the sequence of states A-F-A;
a read ID circuit command to read the digital code in the circuit
breaker, depicted by the sequence of states A-G-A; and a NO OP,
5   depicted by the sequence of states A-H-A. The state delay
associated with state D is to allow the contacts sufficient time to
settle before reading the status of the contacts at state E. The
state delays associated with states B and C are to allow the
contacts sufficient time to react before commencing the settling-
10   time delay of state D. The state delays associated with states E
and F are to provide the gate array with the appropriate timing
response before reporting to the controller with the requested
status.

     While the invention has been particularly shown and described
15   with reference to a few particular embodiments, it will be
recognized by those skilled in the art that modifications and
changes may be made to the present invention described above
without departing from the spirit and scope thereof. For example,
in view of their similarities, many of the components or blocks
disclosed herein may be substituted and/or combined with the
arrangement disclosed in the application entitled, "ELECTRICAL
DISTRIBUTION SYSTEM HAVING MAPPABLE CONTROL INPUTS," supra.

21

What is claimed is:

1. An energy management loadpanel arrangement, comprising:

2   a loadpanel enclosure;

a plurality of circuit breakers secured in the enclosure, at

4   least one of said circuit breakers being digitally-coded and

capable of opening and closing in response to a control signal so

6   as to interrupt an associated current path and capable of providing

a digital signal indicative of a specified type of circuit breaker;

8   and

microcomputer means, responsive to said digital signal, for

10   determining the type of circuit breaker represented by said digital

signal and for generating said control signal to control said at

12   least one circuit breaker and its associated current path.

2. An energy management, loadpanel arrangement, according to

2   claim 1, wherein said digital signal is provided by said at least

one circuit breaker using manually settable bits.

3. An energy management, loadpanel arrangement, according to

2   claim 2, wherein said manually settable bits include soldered

jumper wires.

4. An energy management, loadpanel arrangement, according to

2   claim 2, wherein said at least one circuit breaker further includes

a digital interface circuit, connected to said manually settable

4   bits, for permitting said microcomputer means to read the manually

     settable bits selectively.

     5.   An energy management, loadpanel arrangement, according to

2   claim 4, wherein said digital interface circuit includes a shift

     register.

     6.   An energy management, loadpanel arrangement, according to

2   claim 4, wherein said digital interface circuit indicates the

     number of poles included in said at least one circuit breaker.

     7.   An energy management, loadpanel arrangement, according to

2   claim 1, further including a real-time-clock circuit, coupled with

     said at least one microcomputer means, for automatically providing

4   the time of day to said microcomputer means.

     8.   An energy management, loadpanel arrangement, according to

2   claim 1, wherein said at least one circuit breaker includes a worm

     gear driving means for interrupting the associated current path.

     9.   An energy management, loadpanel arrangement, according to

2   claim 8, wherein the gear driving means includes a motor having a

     shaft which controls a coupling member secured to the movable

4   contact.

23

10. A circuit breaker device for interrupting power in a

2   circuit path between a source and a load in response to a control

    signal from a computer, the circuit breaker device comprising:

4   a first contact and a second contact cooperatively

    arranged in the circuit path so as to provide current from the

6   source to the load and at least one of the contacts being movable

    for interrupting the power provided to the load;

8   means, responsive to open control and closed control

    signals, for moving said at least one movable contact so that the

10 circuit path is interrupted and established, respectively; and

            a digital code circuit for providing a digital signal

12 representing a designated type of circuit breaker; and

            means for programming said digital code circuit to

14 designate that the circuit breaker device is a particular type;

            wherein the computer determines the type of circuit

16 breaker by reading said digital signal and controls the circuit

    breaker device by sending the open control and closed control

18 signals.

    11. A circuit breaker device as claimed in claim 10 wherein

2   the digital code circuit responds to a clock signal by providing an

    output signal for the microcomputer.

    12. A circuit breaker device as claimed in claim 10 wherein

2   the digital code circuit includes parallel to serial conversion

    means.

13. A circuit breaker device as claimed in claim 12 wherein

2   the clock signal and the output signal share a common lead.

14. A circuit breaker device as claimed in claim 12 further

2   including motor and a printed circuit board coupled electrically to

the motor and to the microcomputer.

15. A circuit breaker device as claimed in claim 10 further

2   including a trip mechanism for moving the movable contact to an

open position in response to the presence of an overload condition,

4   and wherein the trip mechanism operates independently of the motor.

16. A remotely controllable circuit breaker device for

2   interrupting power in a circuit path between a source and a load,
comprising:

4   a first contact and a second contact cooperatively
arranged in the circuit path so as to provide current from the

6   source to the load and at least one of the contacts being movable
for interrupting the power provided to the load;

8   means, responsive to open control and closed control
signals generated from a remote location, for moving said at least

10   one movable contact so that the circuit path is interrupted and
established, respectively;

12   a rotatable gear, responsive to said means for moving and
coupled to said at least one movable contact so that the circuit

14   path is interrupted in response to said control signal;

              a digital code circuit for providing a computer-readable

16   digital signal representing a designated type of circuit breaker;
and

18   manually settable means for programming said digital code
circuit to designate that the circuit breaker device is of a

20   particular type.

17. A circuit breaker device as claimed in claim 16 wherein

2   the digital code circuit includes means for providing the computer-
readable digital signal in serial form.

26

18. A circuit breaker device as claimed in claim 17 wherein

2   said means for providing further includes a shift register,
     responsive to a clock signal, for converting an output of said

4   manually settable means into a serial data stream.

19. A circuit breaker device as claimed in claim 17 wherein

2   said means for providing further includes means for receiving a
     clock signal and for generating at least one bit of said computer-

4   readable digital signal on a common data line.

20. A circuit breaker device as claimed in claim 16 wherein

2   the computer-readable digital signal indicates at least one of the
     following: how many poles the circuit breaker device includes, the

4   position of the first and second contacts, current rating of the
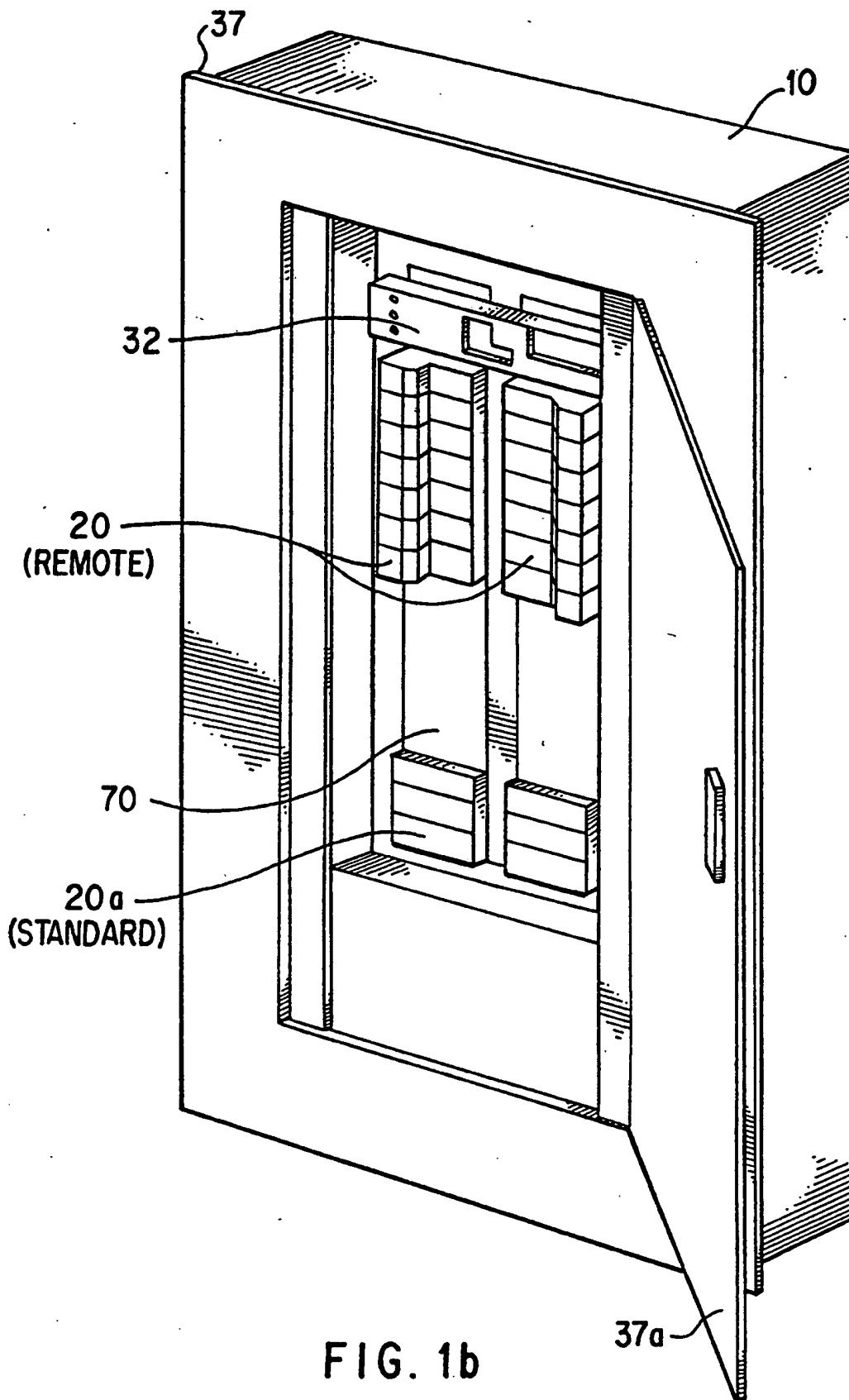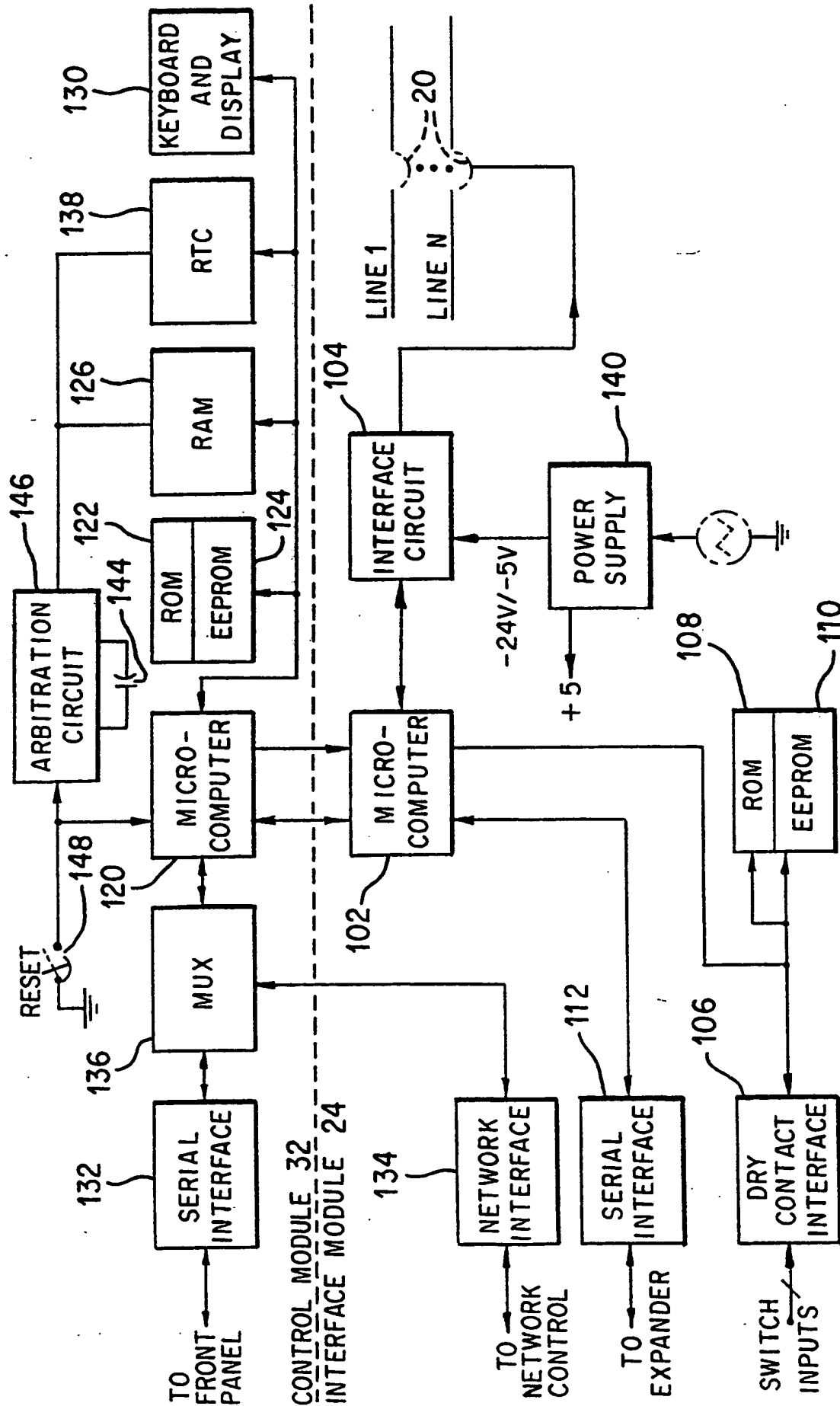   circuit breaker, whether there exists a circuit breaker.

FIG. 1a

FIG. 1b
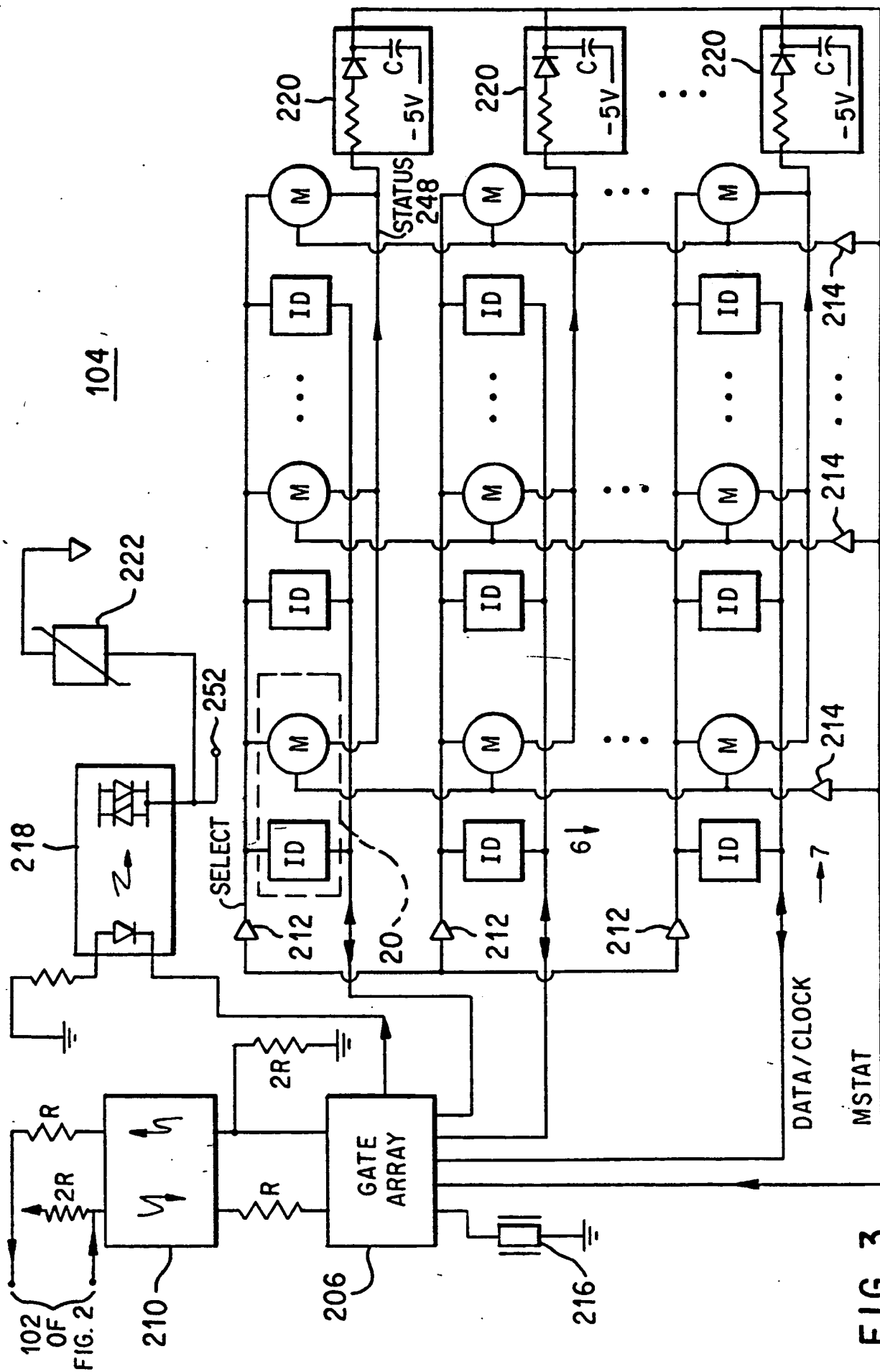
FIG. 2

FIG. 3

FROM
/206

MDO → 6

CDa   3.9R

CDb   0.75R

214

234   235   FROM
16 OR 18

-24V

2.2R

235   10R

-24V   -5V

OPEN   232   250

CLOSE

236

-5V

MSTAT

20R

-5V

FIG. 4

SDO - 7

FROM
206

RDa   3.9R

RDb   0.75R
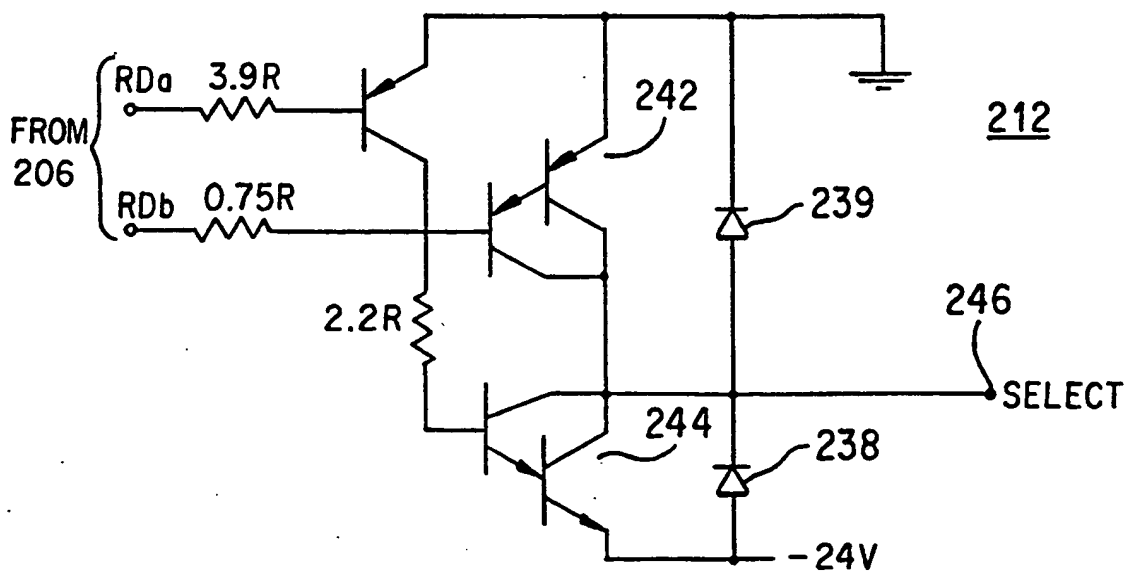
212

242   239

2.2R

246

SELECT

244   238

-24V
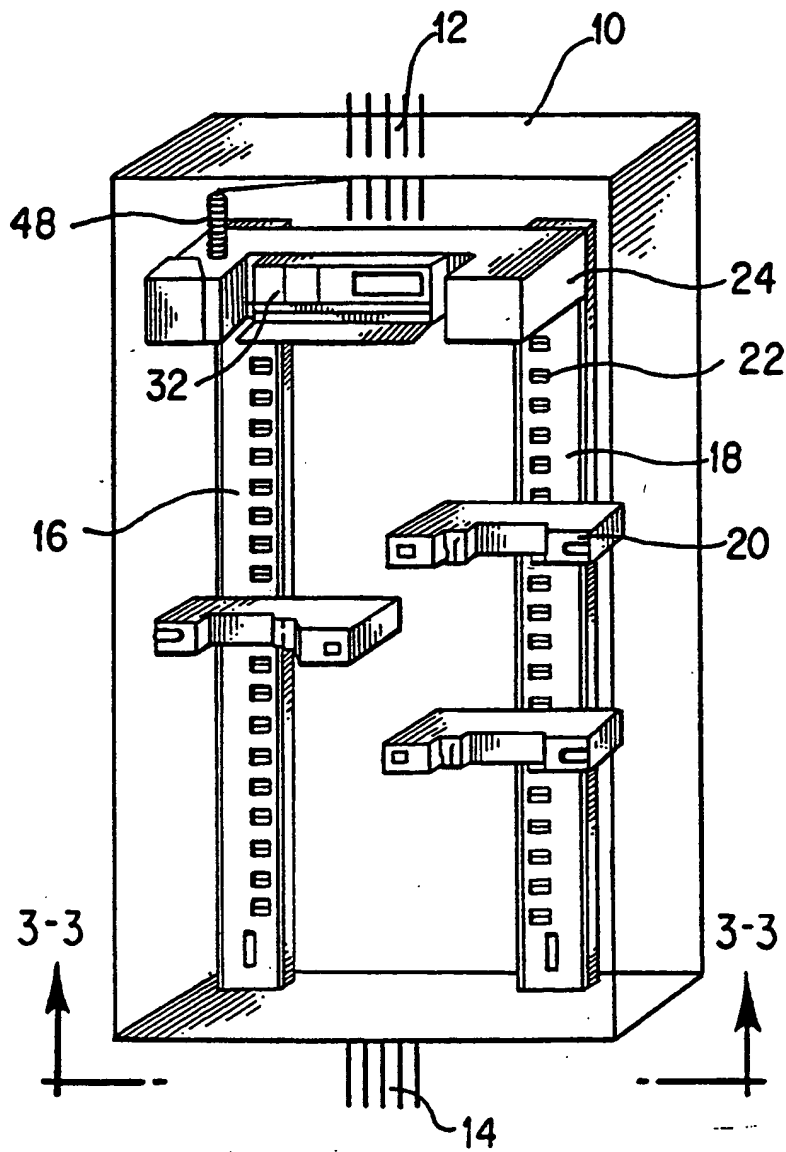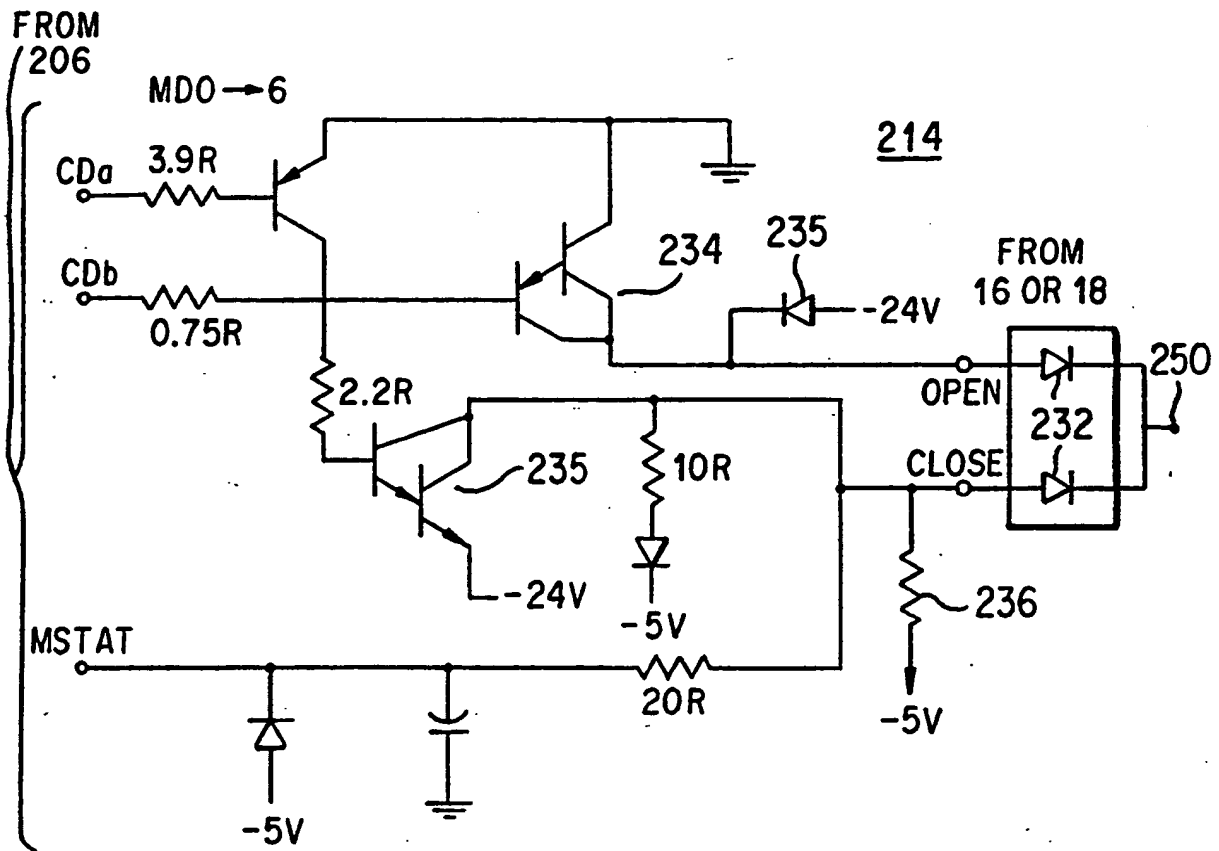
FIG. 5
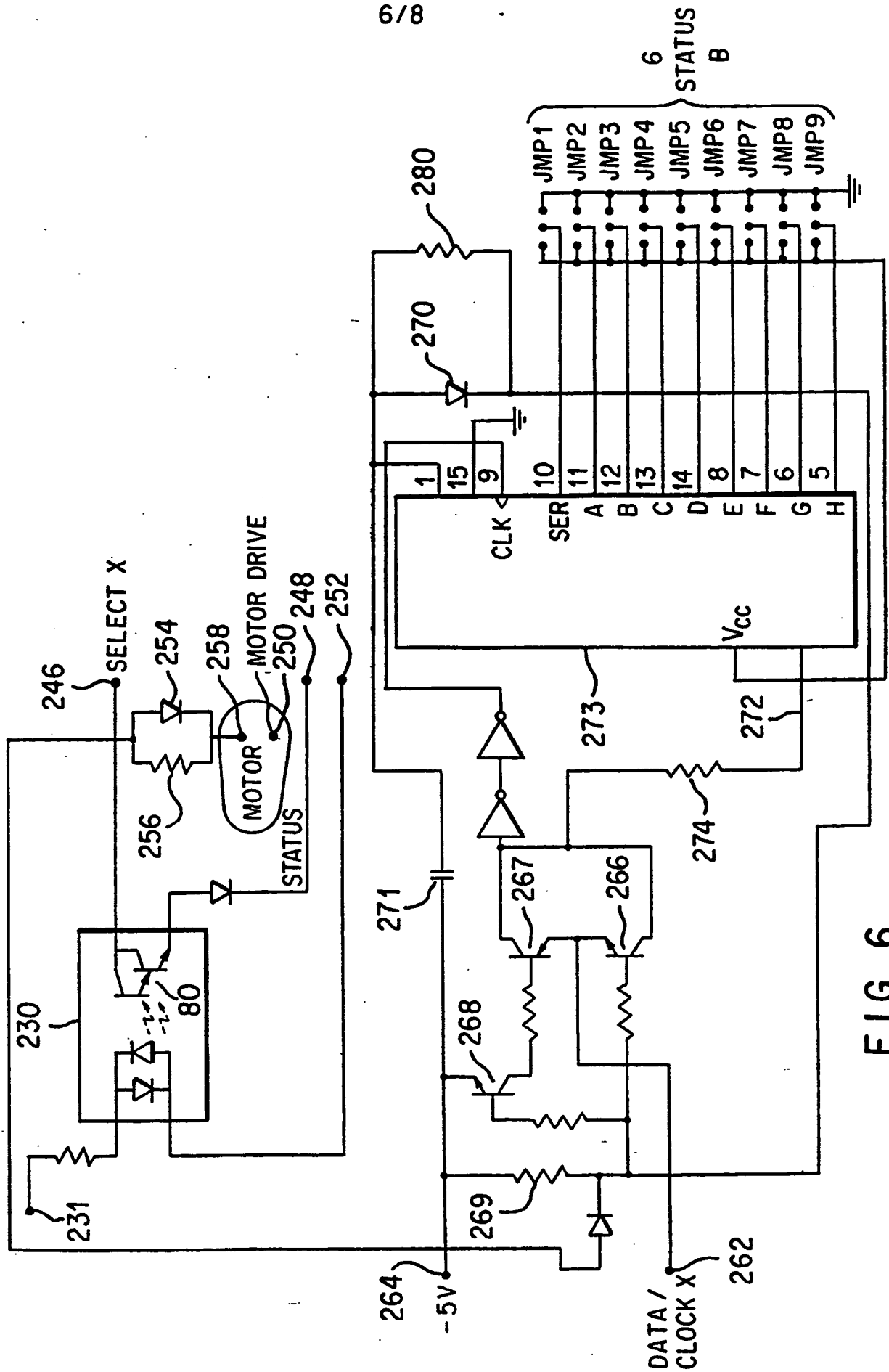
FIG. 6
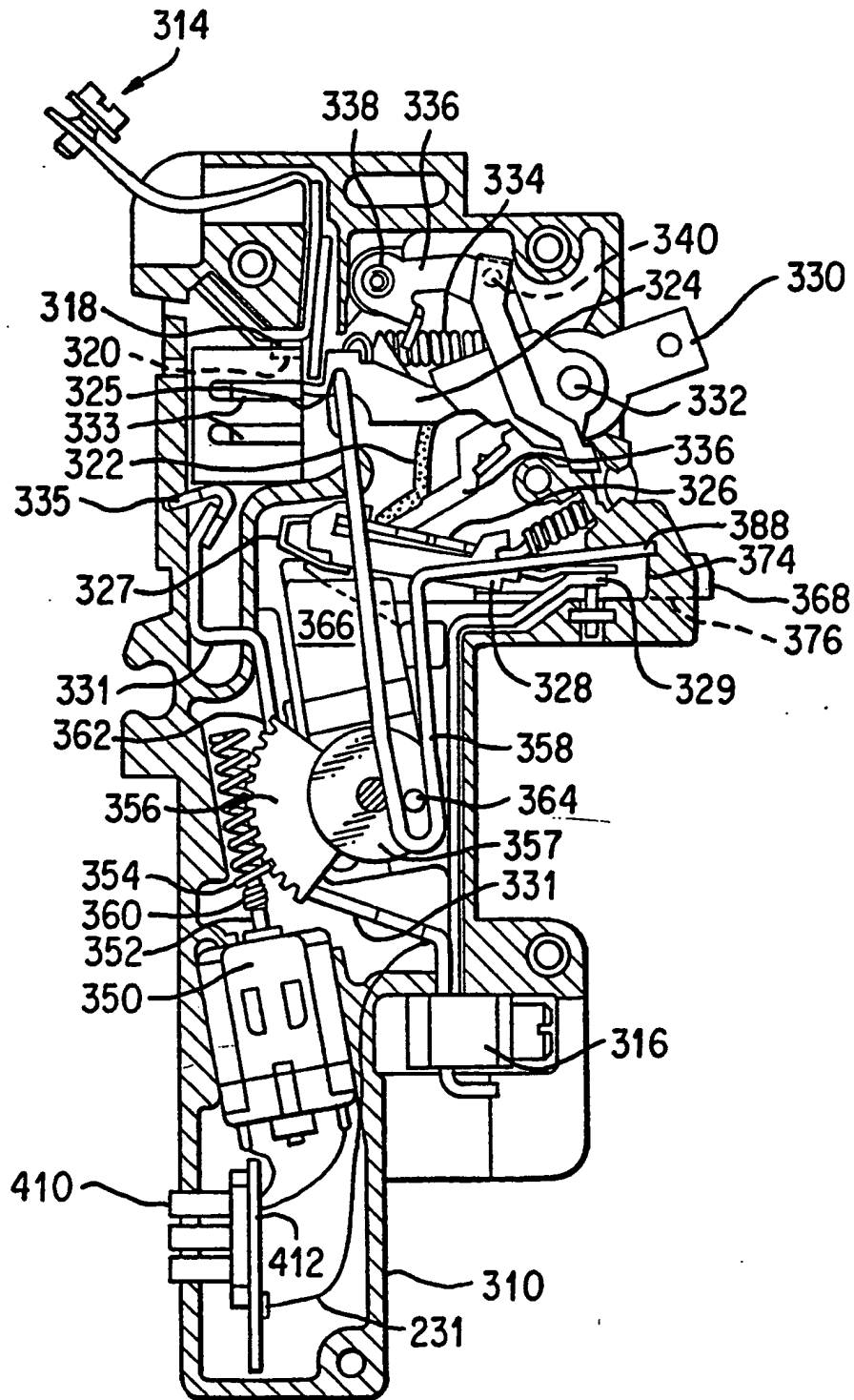
FIG. 7
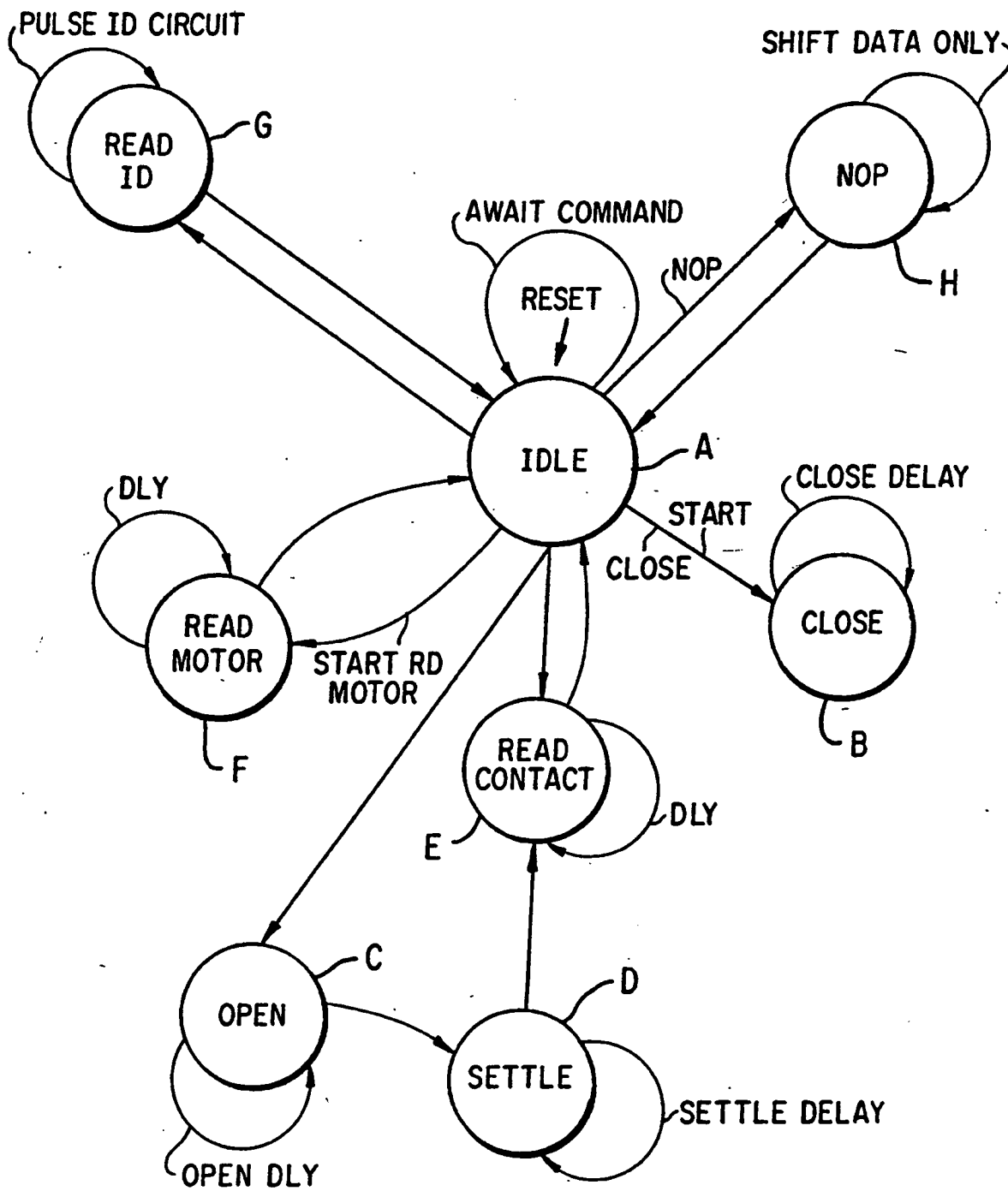
FIG. 8

INTERNATIONAL SEARCH REPORT

	International application No.
	PCT/US93/05984

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) :G06F 15/46
US CL :364/140, 483, 493
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : Please See Extra Sheet.

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US, A, 4,827,369 (Saletta et al) 02 May 1989, col. 5, line 11, col. 18, line 3 to col. 19, line 54.	1-20
Y	US, A, 3,689,887 (La Falce et al) 05 September 1972, col. 2, line 57 to col. 3, line 17.	1-20

☐ Further documents are listed in the continuation of Box C.   ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be part of particular relevance
"E" earlier document published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
04 August 1993	02 SEP 1993

Name and mailing address of the ISA/US	Authorized officer
Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231	JOSEPH F. RUGGIERO
Facsimile No. NOT APPLICABLE	Telephone No. (703) 305-9767

Form PCT/ISA/210 (second sheet)(July 1992)*